Svilen Kanev

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Research interests

My main interests are in the areas of computer systems and architectures. Very broadly, I like exploring hardware-software approaches to lower-level problems, be it reliability to voltage noise, power delivery design, datacenter power management or parallelism.

Education

2012–2016 **School of Engineering and Applied Sciences, Harvard University**
PhD in Computer Science; MS in Computer Science
Advised by Professor David Brooks and Professor Gu-Yeon Wei

2008–2012 **School of Engineering and Applied Sciences, Harvard University**
Bachelor of Arts in Computer Science
Advised by Professor David Brooks, GPA 3.69/4.00

2007–2008 **Faculty of Physics, Sofia University, Bulgaria**
Worked towards a Bachelor of Science in Experimental Physics before moving to Harvard.

Honors and Awards

2015 Siebel Scholar, Class of 2016. *Siebel Foundation* [93 graduate students worldwide]

2015 Communications of the ACM Research Highlight. *Association of Computing Machinery* [10 papers annually]

2012 Outstanding Undergraduate Researcher Award (runner-up). *Computing Research Association* [4 undergraduate students USA-wide]

2011, 2016 Top Picks in Computer Architecture. *Institute of Electrical and Electronic Engineers (IEEE) Micro* [11 papers annually]

2008 Second place. *Bulgarian National College Students Physics Olympiad*

2007, 2006 Silver medal, Bronze medal. *International Physics Olympiad*

2007, 2006 First place, Second place. *Bulgarian National Physics Olympiad*

2002 First place. *Bulgarian National Informatics Olympiad*

Professional experience

Since Sep 2016 **Google** Software Engineer
Performance characterization and optimization.

Jun 2009 – Sep 2016 **Harvard University** Research Assistant, Architecture group under Prof. David Brooks
Various topics on the hardware-software boundary: reliability for voltage variation; power delivery design; power-performance modeling; datacenter applications; automatic parallelization.

Oct 2015 – Jan 2016 **Google** Software Engineering Intern, Languages and platforms group under Dr. Tipp Moseley
Jun 2014 – Nov 2014 At-scale workload characterization and performance opportunities for datacenter applications.

Jun 2013 – Aug 2013 **Google** Software Engineering Intern, Platforms group under Dr. Kim Hazelwood

Jun 2012 – Nov 2012 Investigated power management opportunities for datacenter-scale applications.

Jun 2011 – Aug 2011 **Microsoft Research** Research Intern, Architecture group under Prof. Doug Burger
Worked on the Explicit Datagraph Execution (EDGE) E2 architecture; Evaluated policies related to dynamic core composability and created power models for the architecture.

Jun 2010 – Aug 2010 **Intel** Software Engineering Intern, VSSAD group under Dr. Robert Cohn
Developed a scheme for compressing execution traces which relies on instruction interpretation; Developed a partial IA32 functional simulator as part of the scheme.

Oct 2008 – Jun 2009 **Harvard-Smithsonian Center for Astrophysics** Research Assistant
Developed software to stack X-Ray sources from the Chandra observatory; The software allowed analysis of objects at previously unreachable observation depths.

Sept 2008 – May 2013 **Robotic Football Club (RFC) Cambridge** Software Team Leader
Developed software for the RFC team in Robocup's small-sized league; Led a development team of 5-10 undergraduates; Responsible for a 20-30 KLOC codebase.

Nov 2007 – Aug 2008 **DAVID Holding** Web Developer
Front-end and back-end of a document management system; Developed custom solutions to corporate customers; Optimized the core system to handle heavy enterprise workloads.

Publications

Full list: http://skanev.org/pubs

Mallacc: accelerating memory allocation.
Svilen Kanev, Sam (Likun) Xi, Gu-Yeon Wei, David Brooks
Architectural Support for Programming Languages and Operating Systems (ASPLOS). April 2017.

Profiling a Warehouse-Scale Computer.
Svilen Kanev, Juan Pablo Darago, Kim Hazelwood, Parthasarathy Ranganathan, Tipp Moseley, Gu-Yeon Wei, David Brooks
International Symposium on Computer Architecture (ISCA). June 2015.

Tradeoffs between Power Management and Tail Latency in Warehouse-Scale Applications.
Svilen Kanev, Kim Hazelwood, Gu-Yeon Wei, David Brooks
International Symposium on Workload Characterization (IISWC). October 2014.

HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs.
Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei, David Brooks
International Symposium on Computer Architecture (ISCA). June 2014.

Characterizing and Evaluating Voltage Noise in Multi-Core Near-Threshold Processors.
Xuan Zhang, Tao Tong, Svilen Kanev, Saekyu Lee, Gu-Yeon Wei, David Brooks
International Symposium on Low Power Electronics and Design (ISLPED). July 2013.

XIOSim: Power-Performance Modeling of Mobile x86 Cores.
Svilen Kanev, Gu-Yeon Wei, David Brooks
International Symposium on Low Power Electronics and Design (ISLPED). July 2012.

Portable Trace Compression through Instruction Interpretation.
Svilen Kanev, Robert Cohn
International Symposium on Performance Analysis of Systems and Software (ISPASS). April 2011.

Voltage Smoothing: Characterizing and Mitigating Voltage Noise in a Production Processor Using Software-Guided Thread Scheduling.
Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei, David Brooks
International Symposium on Microarchitecture (MICRO). December 2010.